Low Mismatch Wide Swing Charge Pump for PLLs

Konstantinos Moustakas, Stylianos Siskos
Electronics Lab., Physics Dept.
Aristotle University of Thessaloniki
Thessaloniki, Greece
kmoustak@physics.auth.gr, siskos@physics.auth.gr

Abstract—An accurate, wide output swing, low voltage charge pump is proposed. It is based on a second generation current conveyor which is used to equate charging and discharging currents. A low voltage enhanced current mirror ensures matching between nominal and output currents and current steering is used to minimize charge sharing. Simulation results characterize performance of the proposed circuit.

Index Terms—Charge Pump, Low Mismatch, Low Voltage, Wide Swing, PLL

I. INTRODUCTION

In the recent years there has been an explosive growth in mobile communications and wireless systems. Integrated frequency synthesizers and PLLs enable cheaper and higher quality implementations. Charge pump phase locked loops (CPLLs) are the most widely adopted circuits in wireless applications including transceivers, frequency domain multiplexing and synthesizers because they incorporate simple design combining tradeoff decoupling and theoretically zero static phase offset. In Fig.1 the block diagram of a CPLL is shown. It consists of a phase frequency detector (PDF) to detect the phase error between the reference and the divided feedback signal, a charge pump to charge and discharge the filter capacitor, tuning its voltage according to the PDF UP and DOWN signals and a voltage controlled oscillator (VCO) which output frequency depends on the filter’s tuning voltage $V_{\text{tune}}$.

Charge pump is one of the key components in PLL performance. Mismatch between charging and discharging currents induces FM modulated reference spurs in the output signal and thus must be minimized. Furthermore as supply voltage is becoming lower, low voltage designs must be employed without compromising wide output swing to allow VCO compatibility and flexibility.

II. CHARGE PUMP NON-IDEALITIES

A conventional charge pump, shown in Fig. 2 consists of two current sourcing transistors and two switches. The current sources M1 and M4 are biased by proper constant voltages, and the switches M2 and M3 are driven by the PFD up and down signals.

![Fig. 2. Basic CP structure](image)

Two fundamental problems arise with this design. First PMOS and NMOS devices are inherently unmatched and their properties do not vary with the same coefficients. Second, even if they were matched second order phenomena as channel length modulation alter the drain currents of M1 and M2 as the filter voltage $V_{\text{tune}}$ varies. Thus the drain currents of M1 and M4 are generally not equal and the mismatch current depends on the VCO tuning voltage $V_{\text{tune}}$.

To eliminate the dead zone, short UP and DOWN pulses are produced by the PFD in every cycle. In this short period of time, when the CP current sources are mismatched, a net current is deposited to the filter capacitor. Because of the feedback loop action, within a period the average VCO tuning voltage must be held constant. To compensate for the CP mismatch current, a timing mismatch is created between the UP and DOWN signals in lock state. Thus a charge equal to:

$$ I_{\text{mis}} \cdot t = I_{\text{mis}} \cdot (t_{\text{delay}} - t_{\text{mis}}) \tag{1} $$

is transferred to and from the filter capacitor in every period.

The timing mismatch produces a phase offset between $F_{\text{ref}}$ and $F_{\text{div}}$ [1]:

$$ \Phi = \frac{2\pi}{T_{\text{ref}}} \frac{\Delta I}{T_{\text{c}}} \text{[rad]} \tag{2} $$

![Fig. 1. Charge Pump PLL block diagram](image)
where $\Phi_2$ is the phase offset, $\Delta t_{on}$ is the PFD turn-on time, $T_{ref}$ is the reference signal period, $\Delta_i$ is the CP current mismatch and $I_{CP}$ is the CP nominal output current. The ripples that are present in the tuning voltage produce fm modulation induced reference spurs. Assuming a third order PLL, the spur amount is given by [2], [3]:

$$P_s = 20\log \left( \frac{\sqrt{2} R}{2\pi \times f_{ref}} \times K_{VCO} \right) - 20\log \left( \frac{f_s}{f_p} \right) \text{ [dBc]} \quad (3)$$

where $R$ is the loop filter resistor value, $K_{VCO}$ is the VCO gain and $F_p$ is the filter pole frequency.

### III. Designing a High Performance CP

A state of the art CP used in PLL based integrated systems must combine low voltage operation, very low reference spurs and simple and efficient design. Low voltage operation makes the use of cascode stages improper because of the little voltage headroom. Thus new implementations must be employed to ensure matched charging and discharging currents accompanied with fast switching and low current noise. Various solutions have been proposed using gain boosting stages with operational amplifiers to adjust the biasing voltage of the current sources [3], [4], using only the mosfet switches and extra fine tuning current sources [5], complex $1/\omega^2 k$ parameter independent biasing [6], positive feedback [7] or NMOS only current sources [2].

Current steering in the output stage is very common as a method to improve speed and reduce dynamic glitches and improve transient behavior [2].

In this paper a low voltage wide swing charge pump is proposed. DC current mismatch error is less than 0.1% for an output voltage range of 90mV – 950mV with a voltage supply of 1.1V. It is based on a second generation current conveyor which ensures that the charging current it provides is equal to the discharging current.

### IV. Circuit Description

The proposed circuit is shown in Fig. 3. A low voltage enhanced current mirror composed of mosfets M1, M2, M4 and operational amplifier OP1 is used to set the output current which is $n = \frac{(W/L)_{M2,3}}{(W/L)_{M1}}$ times larger than the bias current. $I_{DM2}$ is steered according to the PFD signals, so M2 remains in the saturation region. When charging M2 is directly connected to the output via M6. When discharging M2 is connected to the X input of the CCII+ via M7 and because $I_X = I_Z$, the charging current equals the discharging current. In tri-state operation, M2 is connected to the X input of the CCII+ via M7 and because $I_X = I_Z$, the charging current equals the discharging current. In tri-state operation, M2 is connected to the X input of the CCII+ via M7 and because $I_X = I_Z$, the charging current equals the discharging current. In tri-state operation, M2 is connected to the X input of the CCII+ via M7 and because $I_X = I_Z$, the charging current equals the discharging current. In tri-state operation, M2 is connected to the X input of the CCII+ via M7 and because $I_X = I_Z$, the charging current equals the discharging current.

$$I_{DM3} = I_X = I_Z, \text{ while } M2 \text{ provides the discharging current. The CCII+ voltage}$$

$$\text{Fig.3. Accurate wide swing charge pump: (a) the proposed circuit, (b) The rail to rail second generation current conveyor used}$$

### V. Simulation Results

The performance of the proposed circuit is assessed via simulations using Cadence Spectre tools in 65nm process. DC mismatch current and dynamic range is compared to three alternative designs of the references [3], [4] and the proposed circuit shown in Fig.3a. In case of the circuit proposed in [4], a DC feedback circuit was used to extend the dynamic range by adjusting the cascode transistor voltage at the drain node.

The reference bias current equals $I_{ref} = 200\mu A$ and the n factor is 4 making the nominal CP current equal to 1mA. The supply voltage $V_{dd} = 1.1V$. Table I shows the DC mismatch error (%) and the dynamic range for 1% maximum error characteristics of the simulated implementations.

<table>
<thead>
<tr>
<th>TABLE I. SIMULATION RESULTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC mismatch (%)</td>
</tr>
<tr>
<td>Dynamic range for 1% maximum error</td>
</tr>
</tbody>
</table>
The DC mismatch current and the charging (PMOS) and discharging (NMOS) currents are plotted against the output voltage $V_o$ and are illustrated in Fig. 4. Transient behavior for half period wide alternating charging and discharging cycles is shown in Fig. 5.

![Fig. 4. Charging (UP), discharging (DN) and mismatch currents](image)

![Fig. 5. Transient behavior: UP, DOWN signals and output current](image)

As observed, the proposed CP incorporates very low static mismatch for the widest output voltage range. Dynamic glitches are also low as seen from the transient simulation.

**VI. CONCLUSION**

An alternative design of a low voltage, low mismatch CMOS charge pump is proposed. Simulation results demonstrate that the this charge pump matches very accurately the charging and discharging currents for an ultra wide dynamic range making it suitable to be used in high performance modern PLL designs.

**ACKNOWLEDGEMENT**

This research is co-financed by Hellenic Funds and by the European Regional Development Fund under the Hellenic National Strategic Reference Framework 2007-2013, according to Contract no. 11SYN_6_100 of the Project “An E-band/mmwave CMOS RFIC/MMIC implementation for future private networks and mobile backhaul radio applications” within the framework “Cooperation 2011”.

**VII. REFERENCES**